Remarks

The Final Office Action dated December 17, 2010, maintained the following rejections: claims 1-2, 4-8, 10-14, 16-18 and 20 stand rejected under 35 U.S.C. § 102(b) over the Sherwood reference ("Predictor-Directed Stream Buffers"); claims 3, 9, 15 and 19 stand rejected under 35 U.S.C. § 103(a) over the Sherwood reference in view of Handy (the Cache Memory Book); and claim 21 stands rejected under 35 U.S.C. § 103(a) over the Sherwood reference in view of Matas ("Memory 1997", Integrated Circuit Engineering Corporation). Applicant traverses all of the rejections and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action. Further, as the rejections are repeated from the previous action, Applicant fully incorporates its traversals of record herein.

Applicant respectfully traverses the §§ 102 and 103 rejections because the Sherwood reference (alone or in combination) lacks correspondence as asserted. For example, the Office Action has not established that the reference(s) teach the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.*, a "stride prediction table" (SPT) that is only accessed in response to a cache miss as claimed. As another example, the Office Action has failed to establish that the cited reference(s) correspond to a stride prediction table that is only updated in response to a cache miss. Because the asserted references fail to teach these (and other) aspects, no reasonable interpretation of the asserted prior art can provide correspondence. As such, the rejections fail.

As applicable to all of the rejections, Applicant submits that the Office Action has mistakenly asserted that portions of the Sherwood reference that refer to a "Markov prediction table," instead apply to a stride table (or "Stride Predictor" as shown in Figure 3). For instance, the Office Action cites to section 4.2 in the Sherwood reference as disclosing limitations directed to only updating a prediction table on a (cache) miss. However, this portion of the Sherwood reference does not refer to a stride table as asserted, but rather refers to a "Markov prediction table." Referring to line 6 of paragraph 2 in section 4.2, the recited "prediction table" refers back to a "Markov prediction table" at lines 3-4 of the same paragraph, and not to the "two-delta stride table" as apparently asserted in the Office Action. This confusion appears to underpin the rejections as applicable to all claims. The following addresses aspects of the

rejections and further explains errors in the rejections as relating to this confusion. Should further clarification be helpful, Applicant invites the Examiner to telephone the undersigned.

With regard to claim limitations directed to "only allowing updates to the SPT in response to the detection of a cache miss," the portions of the Sherwood reference relied upon as corresponding to the claimed "prediction table" do not correspond as asserted. Importantly, the instant Office Action has mistakenly confused Applicant's traversals regarding this matter as being the Applicant's own statements. To assist the Examiner and clarify the record, Applicant notes that its traversals identified errors in the Examiner's assertion that cited discussion in the Sherwood reference referring to a Markov prediction table corresponds to the claimed SPT. To be clear, Applicant did not assert that the Sherwood reference's Markov prediction table is the claimed SPT. On the contrary, Applicant's traversals noted that cited section 4.2 of the Sherwood reference ("[t]he prediction table is only updated on a miss") refers not to the "Stride Predictor," but instead to the "Markov prediction table" as iterated at lines 1-4 of the second paragraph in Section 4.2. This is consistent with the above introductory discussion regarding these mistaken assertions.

Accordingly, the Markov prediction table in the Sherwood reference does not correspond to the claimed stride prediction table and to "only allowing updates to the SPT in response to the detection of a cache miss." The Examiner emphasizes this lack of correspondence in admitting that "the Markov Table *is not* the SPT" (emphasis in original), near the bottom of page 11 of the instant Office Action. Applicant agrees that the cited "Markov prediction table" (with regard to limiting updates to a cache miss) does not correspond to the claimed SPT. The cited portions of section 4.2 thus do not establish correspondence to the claim limitations directed to "only allowing updates to the SPT in response to the detection of a cache miss" as the citations instead refer to the Markov table, which the Examiner has indicated as failing to correspond.

With regard to claim limitations directed to "only allowing accesses to the SPT in response to the detection of a cache miss" (*e.g.*, as in claim 1), the instant Office Action fails to cite any disclosure that provides correspondence to claim limitations as identified in Applicant's traversals. For example, page 11 of the Office Action attempts to respond

to Applicant's traversals regarding these claim limitations by stating that "the rejections are supported with clarifying comments when a citation alone may be unclear." While the relevance or meaning of this response is unclear, it fails to identify any correspondence to limitations directed to "only allowing accesses to the SPT in response to the detection of a cache miss."

As consistent with Applicant's traversals, the cited portions of the Sherwood reference indicating that the "prediction table is only updated on a miss" refer only to a stride update, and do not involve restricting other access. Furthermore, the Sherwood reference uses the asserted "prediction table" as part of a prefetching process that will "run ahead" of data streams, and thus does not restrict accesses only to those responsive to a cache miss. Because of its every-cycle occurrence, this SPT access necessarily occurs at times other than in response to a detected cache miss. The Office Action's assertions that "the rejections are supported" thus fail to establish any disclosure, teaching or suggestion of limitations directed to restricting all access to a prediction table as claimed (and generally fail to completely address Applicant's traversals).

In view of the above and Applicant's repeated traversals of record, Applicant submits that the record as it stands (for Appeal) is insufficient for maintaining the rejection of claim 1, or for maintaining the rejections of independent claims 11, 17 and 21 which are similarly improper for failing to establish correspondence. Applicant therefore requests that the rejections be removed.

Further regarding the rejection of claim 21, page 13 of the Office Action attempts to respond to Applicant's traversals regarding the lack of correspondence to functions carried out in a filter circuit by stating that "the examiner has provided clarifying comments" and that "the level of detail the applicant requires is not clear." Applicant submits that this response fails to address the lack of correspondence, as the Examiner has again failed to point out which portions of the four cited columns correspond to the respective claim limitations. Instead, the Office Action asserts that "[s]ince Claim 21 is a method claim, the filter circuit structure is the elements or group of elements which perform the methods of the claimed filter circuit." Applicant submits that the Office Action has not pointed out any such "elements or group of elements which perform the

methods of the claimed filter circuit." The rejection of claim 21 is therefore improper and should be removed.

With respect to the rejections of claims 6 and 7, which rely upon unsupported assertions of allegedly inherent subject matter, Applicant had submitted evidence (in its previous response) establishing that a cache miss does not necessarily require the operation as asserted in the Office Action. The instant Office Action failed to meet its burden under M.P.E.P. § 2131.01(III) in providing any intrinsic evidence supporting the alleged inherency and establishing that the cited (Sherwood) reference *necessarily* operates as asserted. Accordingly, the rejections of claims 6 and 7 are improper and should be removed.

Regarding the § 103(a) rejections, the instant Office Action fails to overcome Applicant's traversals in failing to provide any explanation or supporting citation as to how the Sherwood reference would function as modified, or as to any motivation for modifying the Sherwood reference as proposed. The Examiner's response at page 15 continues to rely upon an unsupported opinion regarding what one of skill in the art "would recognize" and provides no explanation as to how the circuits in the references would be combined. The Examiner's assertion that "these were clearly provided in the previous rejection" is untenable. Applicant fails to see any such explanation and the Examiner has not explained where any such explanation was provided. With respect to the Examiner's statement that "arguments of counsel cannot take the place of factually supported objective evidence," the relevance of this statement is unclear. Moreover, this statement fails to address Applicant's traversals identifying the Office Action's failure to explain any relationship between the alleged "motivation" and proposed combination at hand (the Office Action itself has provided no objective evidence of such motivation). Accordingly, the § 103(a) rejections have failed to establish correspondence and to meet the requirements of motivation/reason for combining references as asserted under the recent U.S.P.T.O. guidelines and the *KSR* decision.[1] Applicant therefore requests that the § 103(a) rejections be removed.

[1] *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007)

Arguments corresponding to Applicant's traversals of record:

Applicant maintains its traversals of record with respect to the rejections of claim 1-20, as the newly-cited portions of the Sherwood reference fail to overcome the lack of correspondence as established in the record, and overlook aspects of the Sherwood reference that do not support the Office Action's generalizations regarding the alleged teaching in the Sherwood reference. Applicant therefore traverses the § 102(b) and § 103(a) rejections in view of the lack of correspondence in the cited Sherwood reference, either alone or as combined with the Handy reference. For example, the Office Action has failed to establish that the Sherwood reference discloses a "stride prediction table" (SPT) that is only accessed in response to a cache miss as claimed. Because none of the cited references discloses these limitations, the rejections fail.

More specifically, the rejections rely upon a generalized citation to Sections 4.2 and 4.3 of the Sherwood reference (spanning four columns), but do not assert explicit correspondence to limitations directed to limiting all accesses to a SPT by "only allowing accesses to the SPT in response to the detection of a cache miss." While cited Section 4.2, paragraph 2 of the Sherwood reference indicates that the "prediction table is only updated on a miss," this portion refers only to a stride update. None of the cited portions of the Sherwood reference appear to restrict all access to the asserted prediction table (the "Markov Predictor" in Figure 3).

In contrast to the Office Action's assertions, the Sherwood reference appears to access the cited SPT on a regular basis, as the cited "prediction table" is accessed every time a next pre-fetch address is to be generated. Applicant refers the Examiner to page 6 of the Sherwood reference, and the caption under Figure 3, which describes the following:

> To generate the next prefetch address the last address is (1) looked up in the Markov table, and (2) used to calculate a next stride address. If the Markov table hits, then the Markov address is used, otherwise the next stride address is used for the prefetch.

Accordingly, the Markov table (asserted as being the same as the claimed "SPT") is accessed when the next prefetch address is to be generated. This operation is part of a "prefetching" operation to which the entirety of Section 4.2 appears to be directed, as is

also a common theme in the entire Sherwood reference. For instance, referring to the Abstract on the first page, the Sherwood reference recites the following:

> An effective method for reducing the effect of load latency in modern processors is data prefetching. One form of data prefetching, stream buffers, has been shown to be particularly effective due to its' ability to detect data streams and run ahead of them, prefetching as it goes.

In this context, the Sherwood reference uses the cited "prediction table" as part of this prefetching process, which will "run ahead" of data streams.

As consistent with the above-cited caption from Figure 3, the "prediction table" is accessed to suit this need, to prefetch the last address. The Sherwood reference thus does not appear to restrict this access to access responsive only to a cache miss. This is also consistent with Applicant's traversals of record as presented in multiple responses, which noted that Applicant had reviewed other portions of the reference and submited that the Sherwood reference teaches that its SPT is accessed once "each cycle…to make a prediction." Because of its every-cycle occurrence, this SPT access necessarily occurs at times other than in response to a detected cache miss."

The Examiner's previous attempt to overcome Applicant's traversals and this teaching by asserting that the relied-upon portions of the Sherwood reference (Figure 2, Section 4.1) are "a related, but different, system" is clearly in error, as the cited system in Figure 3 operates in the same manner. Moreover, Section 4.1 explicitly recites that "Figure 2 shows the general model of our predictor-directed stream buffer architecture." The discussion in Section 4.1 is clearly applicable to the remaining discussion as it explicitly involves using "priority heuristics described in section 4.4." This is further consistent with the discussion in section 4.2 on page 5, which indicates that the stride table includes both a last and current address and that the stride is calculated by "current miss address – last address." This (non-miss) access appears necessary to the Sherwood reference's purpose as directed to using this difference calculation to store "only the cache misses" in the Markov table (the difference is not stored when the "last address" is not a cache miss). Accordingly, this architecture applies to the disclosed stride table.

In view of the above and Applicant's repeated traversals of record, Applicant submits that the record is insufficient for maintaining the rejection of claim 1, or for maintaining the rejections of independent claims 11, 17 and 21 which are similarly

improper for failing to establish correspondence. For example, the cited portions of the Sherwood reference fail to disclose "a filter circuit preventing both accesses and updates to the SPT unless a cache miss is detected" as in claim 11, or "restricting accesses to the SPT in response to the detection of a cache miss" as in claim 17. Specifically regarding the rejection of claim 21, the Office Action has not established correspondence to a filter circuit that restricts accesses and updates to a SPT as claimed, as consistent with the above discussion. Should the Examiner maintain the rejections as stated, Applicant requests that the Examiner address its traversals regarding this lack of correspondence (doing more than generally citing to four columns of the Sherwood reference, in which Applicant cannot ascertain any teaching supporting the Examiner's position).

Applicant further submits that the rejections of the dependent claims are improper for reasons including those stated above in connection with the independent claims from which they depend. However, the Office Action has also failed to establish correspondence to various dependent claim limitations. For example, with regard to the rejections of claims 6 and 7, the Response to Arguments fails to establish that the Sherwood reference *necessarily* detects a cache miss as claimed, and fails to provide any evidence supporting the Office Action's assertion that the Sherwood reference "requires" the operation as claimed. As is well known, a cache miss can be detected in a number of ways. For instance, cache misses may involve an instruction read miss, data read miss and data write miss, along with different types of misses within these (*see, e.g.*, Adve *et al.*, "Implementing Sequential Consistency In Cache-Based Systems," *Proceedings of the 1990 International Conference on Parallel Processing*, which is attached hereto).

Accordingly and as consistent with Applicant's traversals, the rejections have failed to establish correspondence to the claims in failing to "make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991) (emphasis added). Applicant therefore submits that the rejections thus fail.

Regarding the § 103(a) rejections, Applicant's traversals have not been addressed and thus stand uncontested in the record. Applicant thus maintains its traversals, and submits that the rejection fails to provide any explanation or supporting citation as to how

the Sherwood reference would function as modified, or as to any motivation for modifying the Sherwood reference as proposed. While the rejections are believed improper for the reasons stated above in connection with the § 102 rejections, Applicant thus believes that the rejections are further improper for these reasons as well.

Specifically regarding the § 103(a) rejection of claim 21, Applicant submits that the Office Action has failed to establish correspondence as the rejection provides no explanation as to how the SRAM in the Matas reference would be combined with the memory in the Sherwood reference, as to where the Matas reference discloses a "single-ported" SRAM, or any rationale for the specific modification of the Sherwood reference as proposed. Applicant is left to guess as to how these circuits would be (or could be) combined into any hypothetical embodiment that corresponds. The Office Action has thus failed to meet the requirements as consistent with the recent U.S.P.T.O. guidelines specifying that "[a]ny rationale employed must provide a link between the factual findings and the legal conclusion of obviousness," and also consistent with the KSR decision and M.P.E.P. § 2143.01." As applicable here, the rejection fails to address any such factual findings regarding any modification of the Sherwood reference, in failing to explain how the Matas reference (*e.g.*, the SRAM TFT cell in Figure 8-10) would be implemented as a single-ported SRAM or would be implemented with the buffer architecture in cited Figure 3 of the Sherwood reference. Moreover, the asserted rationale for combining the references (that SRAM is "commonly used" and is "faster and uses less power") is devoid of any explanation relevant to the specific modification at hand, to replace the circuits in the Sherwood reference with the SRAM TFT cell of the Matas reference. Accordingly, the § 103(a) rejection has failed to establish correspondence, and failed to meet the requirements as consistent with the recent U.S.P.T.O. guidelines under the *KSR* decision, referenced above.

In view of the above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, David Schaeffer, of NXP Corporation at (212) 876-6170.

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